

Application No. 10/601,958
June 15, 2004
Page 2

Docket: P910252

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method of programming memory cells of a memory device, the method comprising:
selectively depositing a first insulating layer over a first portion of the memory cells while not depositing the first insulating layer over a second portion of the memory cells; and
selectively depositing a second insulating layers over parts of a first the second portion of the memory cells while not depositing the second insulating layers over parts of a second the first portion of the memory cells, to thereby program the memory device.
2. (Currently Amended) The method as set forth in claim 1, wherein the parts are first and second portions comprise at least one of electrodes, channels and gate electrodes.
3. (Currently Amended) The method as set forth in claim 1, wherein the parts are channels first insulating layer comprises photoresist.
4. (Currently Amended) The method as set forth in claim 1, ~~wherein the parts are gate electrodes~~ and further comprising:
removing the first insulating layer; and
forming a conductive layer to contact the first portions.
5. (Currently Amended) The method as set forth in claim 4, wherein:
the memory cells are transistors;
the first and second portions are gate electrodes;

Application No. 10/601,958
June 15, 2004
Page 3

Docket: P910252

word lines extend over the gate electrodes;
gate electrodes of the ~~first~~ second portion of the memory cells are not connected to the word lines; and
gate electrodes of the ~~second~~ first portion of the memory cells are connected to the word lines.

6. (Currently Amended) A method of programming a memory device having a plurality of memory cells positioned to be coupled to corresponding word lines, the method comprising masking and subsequently coupling only predetermined ones of the plurality of memory cells to their corresponding word lines and leaving other memory cells of the plurality of memory cells relatively decoupled from their corresponding word lines.

7. (Currently Amended) The method as set forth in claim 6, wherein:
the masking of the predetermined ones of the plurality of memory cells is followed by unmasking of the predetermined ones of the plurality of memory cells to enable them to be coupled to their corresponding word lines;
the predetermined ones of the plurality of memory cells are not disabled; and
the other memory cells of the plurality of memory cells are disabled.

8. (Original) The method as set forth in claim 6, wherein insulating layers are disposed between the relatively decoupled memory cells and their corresponding word lines, but are not disposed between the coupled memory cells and their corresponding word lines.

9. (Original) The method as set forth in claim 8, wherein:
each memory cell comprises a transistor having two source/drain regions and a gate;
and
the insulating layers are disposed between gates of the relatively decoupled memory cells and their corresponding word lines.

Application No. 10/601,958
June 15, 2004
Page 4

Docket: P910252

10. (Original) The method as set forth in claim 6, wherein substantially all of the memory cells of the memory device have substantially the same threshold voltages.
11. (Original) The method as set forth in claim 6, wherein substantially none of the memory cells of the memory device are ion-implantation coded.
12. (Original) A memory device fabricated according to the method of claim 6.
13. (Currently Amended) A method of programming a memory device comprising disabling predetermined memory cells of the memory device by electrically insulating the predetermined memory cells from word lines of the memory device to which the predetermined memory cells would otherwise be electrically coupled but for the disabling, whereby non-disabled memory cells of the memory device are first masked and then not insulated from, or are insulated to a lesser extent from, corresponding word lines of the memory device.
14. (Original) The method as set forth in claim 13, wherein a first portion of memory cells corresponding to a word line are disabled and a second portion of memory cells corresponding to the same word line are not disabled.
15. (Original) The method as set forth in claim 13, wherein insulating layers are disposed between channels of the disabled memory cells and their corresponding word lines, but are not disposed between channels of the non-disabled memory cells and their corresponding word lines.
16. (Original) The method as set forth in claim 13, wherein:
 - each memory cell comprises a transistor having two source/drain regions and a gate;
 - insulating layers are disposed between gates of the disabled memory cells and their corresponding word lines; and
 - insulating layers are not disposed between gates of the non-disabled memory cells and their corresponding word lines.

Application No. 10/601,958
June 15, 2004
Page 5

Docket: P910252

17. (Currently Amended) The method as set forth in claim 13, wherein the method further comprises:

- providing a substrate having a first surface;
- creating a dielectric layer on the first surface of the substrate;
- forming a plurality of substantially parallel strip-stacked layers on the dielectric layer, each strip-stacked layer comprising a disposable layer formed on a gate electrode layer, the gate electrode layer of each strip-stacked layer being disposed on the dielectric layer;
- forming a plurality of source/drain regions in the substrate, each source/drain region being adjacent to the first surface of the substrate, wherein each strip-stacked layer is disposed substantially between a pair of adjacent source/drain regions;
- forming a plurality of first spacers on the dielectric layer, each of the first spacers being disposed between two adjacent strip-stacked layers;
- patternning the strip-stacked layers to form a plurality of gate electrodes disposed on the dielectric layer and a plurality of disposable pillars disposed on the gate electrodes, wherein portions of the strip-stacked layers are removed thereby creating a plurality of apertures;
- forming a plurality of second spacers within the apertures; and
- removing the plurality of the disposable pillars to form a plurality of openings that expose the plurality of gate electrodes;
- wherein the masking of non-disabled memory cells comprises forming a patterned mask to cover the gate electrodes corresponding to active code positions of the memory device in accordance with the code; ~~and~~
- wherein the disabling of predetermined memory cells further comprises depositing insulating layers on the gate electrodes corresponding to inactive code positions of the memory device in accordance with the code, removing the patterned mask, and forming a plurality of word lines interconnecting the gate electrodes corresponding to the active code positions, each word line being disposed substantially perpendicularly to the source/drain regions, the gate electrodes

Application No. 10/601,958
June 15, 2004
Page 6

Docket: P910252

corresponding to the inactive code positions being electrically isolated from the word lines.

18. (Original) The method as set forth in claim 17, wherein:
portions of the first spacers are removed during the step of patterning; and
the forming of a plurality of second spacers comprises forming a plurality of second spacers in place of at least the portions of the first spacers that have been removed.
19. (Original) The method as set forth in claim 18, wherein:
the forming of a plurality of substantially parallel strip-stacked layers comprises forming a plurality of polysilicon gate electrode layers and a plurality of silicon nitride disposable layers;
the depositing of insulating layers comprises spin-on coating silicon dioxide insulating layers;
the forming of a patterned mask comprises forming a patterned photoresist mask;
the forming of a plurality of first spacers comprises forming a plurality of first silicon dioxide spacers; and
the forming of a plurality of second spacers comprises forming a plurality of second silicon dioxide spacers.
- 20-30. Cancelled.